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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,652	01/18/2002	Ronalf Kramer	1406/36	5317
25297	7590	04/26/2004	EXAMINER	
JENKINS & WILSON, PA			TAN, VIBOL	
3100 TOWER BLVD			ART UNIT	PAPER NUMBER
SUITE 1400				
DURHAM, NC 27707			2819	

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,652	KRAMER, RONALF	
	Examiner Vibol Tan	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 03 March 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1 and 3-17 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,3-11,15-17 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

1. In view of the Appeal Brief filed on 03/03/2004, PROSECUTION IS HEREBY REOPENED. The new ground of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
- (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Objections

2. Claim 6 is objected to because of the following informalities: change "a negative signal pulse at the output terminal" to "the negative signal pulse (logic 0) at the output terminal". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizukami et al. (U. S. PAT. 5,111,080).

In claim 6, Mizukami et al. teaches all claimed features in Fig. 3, a circuit for generating a negative signal pulse in response to receiving a sequence of a positive and (logic 1) negative control pulse (logic 0), the circuit comprising: a first transistor (Q1) including a control terminal (the gate terminal) and a load path (a path between node c and VDD) connected between an output terminal (c) and a first supply potential (VDD) for receiving a negative control pulse (Logic 0) at the control terminal; a second transistor (Q2) including a control terminal (the gate terminal) and a load path (a path between node c and ground) connected between the output terminal (c) and a second supply potential (ground) having a potential less than the first supply potential for receiving a positive control pulse (logic 1) at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and a pull-up resistor (R4) connected between the first supply potential (VDD) and the output terminal (c) for generating the negative signal pulse (logic 0) at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

Claim 9 corresponds to detailed circuitry already discussed similarly with regard to claim 6.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 3, 7, 8, 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizukami et al. (U. S. PAT. 5,111,080) in view of Proebsting (U. S. PAT. 5,926,050).

In claim 1, Mizukami et al. teaches all claimed features in Fig. 3, a circuit for generating a single asynchronous signal pulse at an output of an integrated circuit (Fig. 3), the circuit comprising: an integrated circuit comprising a push-pull driving circuit (Q1, Q2) having a first and second transistor (Q1, Q2) including control terminals (gate terminals) being independently controlled by different control pulses (output from N1 for Q1 and output from N2 for Q2) between a first and second supply potential (VDD and ground), and a centre tap (a) connected with an output terminal (c) of the integrated circuit; and a single resistor (R4) being externally coupled with the output terminal of the integrated circuit and being of a pull-up (as shown) or pull-down type, wherein the type of the resistor determines, by application of a first control pulse (when IN is low, thus low voltage level is at the terminal of Q2) on the control terminal of the second transistor and then a second control pulse (when IN is high, thus high voltage level is at the terminal of Q1) on the control terminal of the first transistor, whether a single positive (IN) or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal; with the exception of teaching wherein a waiting time is provided between the first control pulse and the second control pulse such that the two pulses do not overlap. However, Proebsting teaches in Figs. 1 and 2, a waiting time ($\Delta t_2 - \Delta t_1$) is provided between the first control

pulse (26') and the second control pulse (26'') such that the two pulses do not overlap (as shown).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the circuit of Mizukami et al. with the teachings of Proebsting wherein two pulses having the waiting time such that do not overlap, in order to ensure that one signal will arrive to condition a circuit before the other, and that the second transition of the second signal to arrive before that of the first signal.

In claim 3, Mizukami et al. further teaches wherein one of the two control pulses is generated from the other of the two control pulses by an inverter delay device (IN1).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to to combine the circuit of Mizukami et al. with the teachings of Proebsting wherein two pulses having the waiting time such that do not overlap, in order to ensure that one signal will arrive to condition a circuit before the other, and that the second transition of the second signal to arrive before that of the first signal.

In claim 7, Mizukami et al. teaches all claimed features in Fig. 3; with the exception of teaching wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap. However, Proebsting teaches in Figs. 1 and 2, a waiting time ($\Delta t_2 - \Delta t_1$) is provided between the first control pulse (26') and the second control pulse (26'') such that the two pulses do not overlap (as shown).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the circuit of Mizukami et al. with the teachings of

Proebsting wherein two pulses having the waiting time such that do not overlap, in order to ensure that one signal will arrive to condition a circuit before the other; and that the second transition of the second signal to arrive before that of the first signal.

In claim 8, Mizukami et al. further teaches wherein one of the two control pulses is generated from the other of the two control pulses by an inverter delay device (IN1).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the circuit of Mizukami et al. with the teachings of Proebsting wherein two pulses having the waiting time such that do not overlap, in order to ensure that one signal will arrive to condition a circuit before the other, and that the second transition of the second signal to arrive before that of the first signal.

Claims 10 and 11 are essentially the same scope of claims 7 and 8. Therefore, they are rejected similarly.

4. Claims 4-5 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizukami et al. in view Proebsting and further in view of Taguchi (U. S. PAT. 6,160,417).

In claim 4, Mizukami et al. in view of Proebsting teaches all claimed features of claim 1, as explained above; with the exception wherein the first transistor is a P-channel MOS transistor and the second transistor is an N-channel MOS transistor. However, Taguchi teaches in Fig. 3 wherein the first transistor (13) is a P-channel MOS transistor and the second transistor (14) is an N-channel MOS transistor, the control connection (the gate electrode) of the first transistor (13) being inverted (PMOS transistor inherently having inverting gate electrode).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to form a push-pull circuit by selecting two different types of transistors instead of using same types of transistors as shown in Fig. 3, Mizukami et al. in order to not having to use an inverter gate circuit to invert the control pulse to appropriately control the push-pull circuit.

In claim 5, Taguchi further teaches in Fig. 3, the circuit as claimed in claim 4, wherein the first transistor (13) and the second transistor (14) form a CMOS inverter (12) with independent control gate connections (separate gate electrodes).

In claim 15, Taguchi further teaches in Fig. 3, the circuit of claim 1, wherein the first and the second transistors (13, 14) include a source and drain, the drain of the first transistor being connected to the drain of second transistor (as shown in Fig. 3 of Taguchi), the source of the first transistor being connected to the first power potential (VCC), and the source of the second transistor being connected to the second supply potential (ground).

In claim 16, Taguchi further teaches in Fig. 3, the circuit of claim 6, wherein the first and the second transistors (13, 14) include a source and drain, the drain of the first and second transistors being connected to the output terminal (6), the source of the first transistor being connected to the first supply potential (VCC), and the source of the second transistor being connected to the second supply potential (ground).

In claim 17, Taguchi further teaches in Fig. 3, the circuit of claim 9, wherein the first and the second transistors (13, 14) include a source and drain, the drain of the first and second transistors being connected to the output terminal (6), the source of the first

transistor being connected to the first supply potential (VCC), and the source of the second transistor being connected to the second supply potential (ground).

Claims 12-14 are not entered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan



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